Patent Claims

1. An amplifier comprising amplification means (AM) comprising an input and an output,

said amplification means (AM) comprising a switching output stage delivering at least one output signal (OUS) via said output,

said amplification means being fed by power supply means (PSM)

said amplifier further comprising compensation means (CM) providing a compensation signal (CS) derived from the power supply voltage (PSV) of the power supply means (PSM), said compensation signal (CS) comprising a substantially inverse representation of said power supply voltage (PSV) and

said compensation signal (CS) being fed to said amplification means (AM).

2. An amplifier according to claim 1, wherein said substantially inverse representation of the power supply voltage (PSV) is scaled by a ratio substantially corresponding to a desired amplification between the output and the input of the amplification means (AM).

3. An amplifier according to claim 1 or claim 2, wherein said compensation signal is established for maintaining a substantially fixed utility area of a period of the amplified pulse width modulated signal regardless of changes in the power supply voltage (PSV).

4. An amplifier according to any of the claims 1 to 3, wherein said compensation means further comprises extrapolation means (EM) adapted for modifying said compensation signal (CS) according to a predefined extrapolation algorithm.

5. An amplifier according to any of the claims 1 to 4, wherein said compensation signal (CS) is established on the basis of an inverting generator (CM) fed by a power supply comprising a circuit adapted for establishing an inverse signal of the voltage of said power supply.

6. An amplifier according to any of the claims 1 to 5, wherein said inverting generator comprises at least one feedback loop having a power supply voltage dependent feedback.

7. An amplifier according to any of the claims 1 to 6, wherein said inverting generator comprises
at least one forward path (LF, MM, QM) having an input and an output,
at least one reference oscillator (SG)
at least one feedback path derived from said forward path and fed back to said input of said forward path by means of a summing point (SP) subtracting the feed-back signal from an input received from said reference oscillator (SG)
wherein said feedback path comprises a power supply voltage dependent feedback

8. An amplifier according to any of the claims 1 to 7, wherein said inverting generator outputs a digital signal on the output (PWCS) of said forward path derived from at least one analog signal received in said input (PSVR).

9. An amplifier according to any of the claims 1 to 8, wherein said forward path comprises a limiter (MM) adapted for providing a pulse width modulated output signal of said forward path.

10. An amplifier according to any of the claims 1 to 9, wherein said forward path further comprises a time quantizer (QM) converting said pulse width modulated signal, preferably two level, into a time discrete signal fed to the output (PWCS) of said forward path.

11. An amplifier according to any of the claims 1 to 10, wherein said compensation signal is fed to said amplification means via at least one multiplication point (MP) in which the compensation signal is multiplied with a preferably digital input signal (IUS).

12. An amplifier according to any of the claims 1 to 11, wherein said compensation means further comprises decimation means (DM) adapted for transforming said compensation signal (CS) into compatibility with said input signal (IUS).

13. An amplifier according to any of the claims 1 to 12, wherein the signal processing performed by said amplification means multiplicatively depend on the power supply voltage.

14. Method for compensating errors of a power signal (PS) comprising a power supply voltage (PSV), comprising the steps of

performing multiplicatively power supply voltage dependent signal processing on an input utility signal (IUS) by means of amplification means (AM),

establishing a compensation signal (CS) comprising a representation of the ratio between a desired voltage (DV) and said power supply voltage (PSV), and

applying said compensation signal (CS) to said input utility signal (IUS) by means of multiplication.

15. Method for compensating errors of a power signal according to claim 14, whereby said establishment of a compensation signal (CS) comprises the steps of
establishing a forward path fed by a reference signal (RS),
establishing a negative feedback path from the output (PWCS) of said forward path, and
scaling the signal of said feedback path proportionally with a representation (PSVR) of said power supply voltage (PSV).

16. Method for providing a reciprocated signal, comprising the steps of
providing an electrical signal (PSVR),
providing at least one feedback loop comprising
at least one forward path comprising at least one non-linearity (MM) and
at least one feedback path comprising at least one variable amplifier (BM),
feeding to at least one of said at least one variable amplifier said electrical signal (PSVR).

17. Method for providing a reciprocated signal according to claim 16, whereby at least one of said at least one forward path is fed with at least one reference signal (RS).

18. Method for providing a reciprocated signal according to claim 16 or claim 17, whereby at least one of said at least one feedback loop comprises at least one quantization means (QM).

19. Method for providing a reciprocated signal according to any of the claims 16 to 18, whereby at least one of said at least one feedback loop comprises at least one digital-to-analog conversion means (DAC).

20. Method for providing a reciprocated signal according to any of the claims 16 to 19, whereby quantization noise introduced at least one of said at least one quantization means (QM) is shaped by at least one loop filter (LF).

21. Method for providing a reciprocated signal according to any of the claims 16 to 20, whereby said reference signal (RS) is an oscillating voltage signal.

22. Method for providing a reciprocated signal according to any of the claims 16 to 21, whereby said non-linearity (MM) is a limiter.

23. Method for providing a reciprocated signal according to any of the claims 16 to 22, whereby said non-linearity (MM) is a comparator.

24. Electrical signal reciprocator (CM) establishing at least one reciprocated electrical signal (PWCS), said electrical signal reciprocator comprising at least one feedback loop, said at least one feedback loop comprising
at least one forward path being fed by a reference signal (RS) and comprising at least one non-linearity (MM), and
at least one feedback path comprising at least one variable amplifier (BM),
wherein at least one of said at least one variable amplifier is controlled on the basis of an electrical signal (PSVR).

25. Electrical signal reciprocator (CM) according to claim 24, wherein at least one of said at least one feedback loop comprises at least one quantization means (QM).

26. Electrical signal reciprocator (CM) according to claim 24 or claim 25, wherein at least one of said at least one feedback loop comprises at least one digital-to-analog conversion means (DAC).

27. Electrical signal reciprocator (CM) according to any of the claims 24 to 26, wherein at least one of said at least one feedback loop comprises at least one loop filter (LF).

28. Electrical signal reciprocator (CM) according to any of the claims 24 to 27, wherein at least one of said at least one forward path further comprises at least one analog-to-digital converter (QM), preferably comprising at least one latch, and at least one of said at least one feedback path comprises at least one digital-to-analog converter (DAC).